# *Impact of etch stop layer on negative bias illumination stress of amorphous Indium Gallium Zinc Oxide transistors*

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***Abstract*—In this work we show that the negative bias illumination stress (NBIS) of amorphous Indium Gallium Zinc Oxide (a-IGZO) transistors with an etch stop layer (ESL) deposited by physical vapor deposition (PVD) is substantially better than the NBIS of devices where the ESL layer is deposited by plasma enhanced chemical vapor deposition (PECVD). Both devices show similar transistor characteristics and bias stress in the dark but under NBIS conditions at 425 nm, PVD ESL based transistors show much less threshold voltage shift. The reduction in deep defects due to passivation by PVD layer is responsible for improved performance under NBIS.**

***Keywords—a-IGZO;ESL;NBIS; PECVD;PVD***

## I. INTRODUCTION

Thin film transistors (TFTs) based on a-IGZO have been extensively researched as an alternative for amorphous silicon and low-temperature polycrystalline silicon in the display industry. High mobility, large-area uniformity and low temperature processing [1] are few of the qualities which make a-IGZO TFTs suitable for active matrix liquid crystal displays (LCD) and organic light emitting diodes (OLED) based displays. However, the instability of oxide devices under electrical bias, temperature dependent and light dependent bias is still an issue. Several approaches have been tried to circumvent this issue. One essential thing is passivation of the TFTs to prevent the interaction of IGZO with the surrounding environment. Moisture and oxygen from the ambient air play an important role in causing the threshold voltage shift. Also passivation helps in protecting the back surface of a-IGZO from damage during the source/drain etch process [2-3]. Plasma enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD) are two techniques used for obtaining the passivation layer, each with their pros and cons. PECVD $SiO_2$ is commonly used as etch-stop-layer (ESL) in the Flat-Panel-Display (FPD) industry as it offers many advantages like high uniformity, good step coverage and high deposition rate. However, at temperatures below 200˚C the density of PECVD layers decreases and there is an increase in the amount of hydrogen incorporated in the a-IGZO. This makes the IGZO highly conductive and the ability to deplete the TFT is lost [4]. Few research groups have demonstrated use of PVD $SiO_2$ [5] or PVD $Al_2O_3$ [6] as passivation layer. PVD dielectrics intrinsically contain less hydrogen, but without modifying the classical process, the uniformity and deposition rates are not satisfactory. However, mf-PVD $Al_2O_3$ layers have been demonstrated with sufficient uniformity and deposition rates up to Gen8 production processes [7]. Both PECVD and PVD cause plasma induced damage to the TFTs. Although the TFT properties can be recovered by thermal annealing some damage will still persist. In this paper we compare electrical bias and light bias stability of PECVD and PVD etch stop layer (ESL) based TFTs. We show that PVD ESL is a better choice for TFTs as the impact of the layer on the TFTs performance is less compared to PECVD layers even though TFT characteristics like mobility and subthreshold slope are similar in both cases.

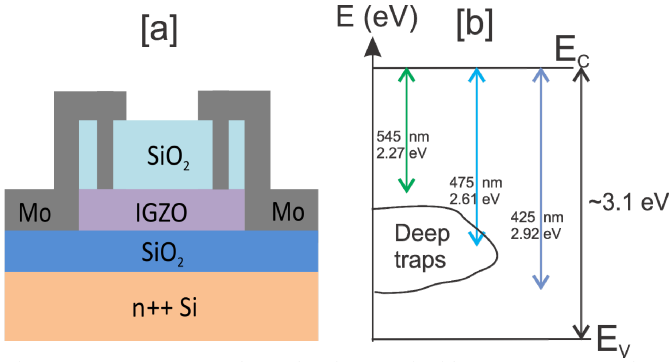


Fig 1: [a] TFT structure under study. $SiO_2$ ESL is either PECVD or PVD layer. [b] schematic energy diagram and the wavelengths (energy) used for NBIS experiments.

## II. EXPERIMENTAL

Bottom gate inverted staggered TFTs were used in this study. Highly doped silicon substrate was used as gate electrode with thermal $SiO_2$ (120 nm) as gate dielectric. a-IGZO layer was deposited by dc sputtering at room temperature (RT) using a-IGZO target (In :Ga : Zn = 1 : 1: 1 atomic%). Following this two different kinds of ESL, both 100 nm thick, were deposited. One was PECVD Silicon dioxide ($SiO_2$) layer at 300°C and the other was deposited by mf-PVD of Silicon at room temperature in $O_2$ atmosphere. Then, the ESL/a-IGZO stack was patterned by a combination of dry etch (using CF4 chemistry) and wet etch (using oxalic acid). This was followed by contact opening by dry etch. S/D contacts were formed by

Molybdenum (Mo) sputtering and dry etch. All layers were patterned by standard photolithography (Fig 1.[a]).
The samples were subjected to thermal annealing at 165 °C in $N_2$ ambient. The Current-Voltage ($I_{ds}$-$V_{gs}$) characteristics of the TFTs were measured using an Agilent 4156 parameter analyzer in air. For negative bias illumination stress light emitting diodes (LEDs) of 545 nm (2.27 eV), 475 nm (2.61 eV) and 425 nm (2.92 eV) were used (Fig 1.[b]). The photon flux was kept constant at $10^{16}$ $cm^{-2}s^{-1}$ and the gate bias voltage ($V_{GS} - V_{on}$) was at -14 V with both source and drain at 0V. Light was switched off during the IV sweep. $V_{ds}$ during measurement was 0.5V. $V_{on}$ is the voltage at which $I_{ds}$ = 100 pA

## III. RESULTS AND DISCUSSION

Initial $I_{ds}$-$V_{gs}$ curves for both the PECVD ESL based TFTs (device A) and PVD ESL based TFT (device B) are shown in Fig 2. After ESL deposition both devices were completely turned on (data not shown). To recover the characteristics they were annealed at 165°C. The characteristics of device A and B are listed in Table 1 (a range is shown from data obtained on 8 TFTs per sample).

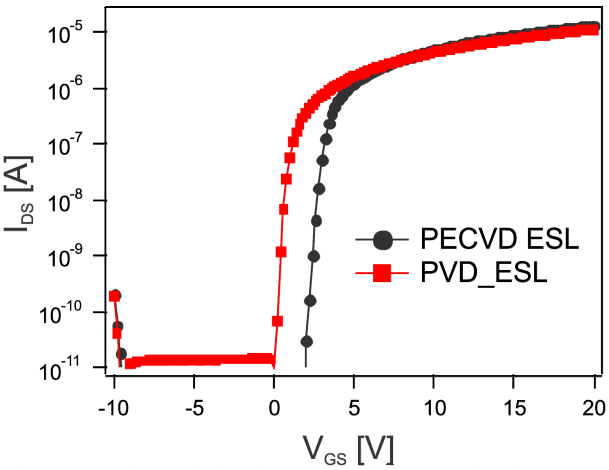


Fig 2: $I_{ds}$-$V_{gs}$ characteristics of PECVD and PVD ESL based TFTs.

Table 1. TFT parameters for PECVD and PVD ESL TFTs

| | **Subthreshold Slope [V/dec]** | **Mobility [$cm^2$/V.s]** | **$V_{TH}$ [V]** |
|---|---|---|---|
| **PECVD ESL** | 0.2-0.25 | 16-17 | 4-5 |
| **PVD ESL** | 0.25-0.3 | 18-19 | 4-5 |

Negative bias stress (NBS) date for both devices are shown in Fig 3.[a] and Fig 4.[a] . The shift in IV curves under NBS conditions for both devices are similar. However, a significant difference is seen under NBIS conditions as shown in Fig 3 and 4. Device A shows higher degradation compared to device B (Fig.5). The maximum shift under the applied NBIS conditions is -13.1 V for device A and -3.1 V for device B at 425 nm. The onset of NBIS shift for device A is also at a higher wavelength (at 545 nm. data not shown). Device B shows a minor shift even at 475 nm. The origin of NBIS shift is associated with deep traps near valance band maximum (VBM) caused by oxygen vacancies ($V_O$) [8]. According to [9] these near VBM states are denser in the surface layer of a-IGZO channel (air or ESL/a-IGZO interface). These states are affected by the environment and to prevent this a passivation layer is used. However, the passivation layer itself leads to some instabilities in device performance.

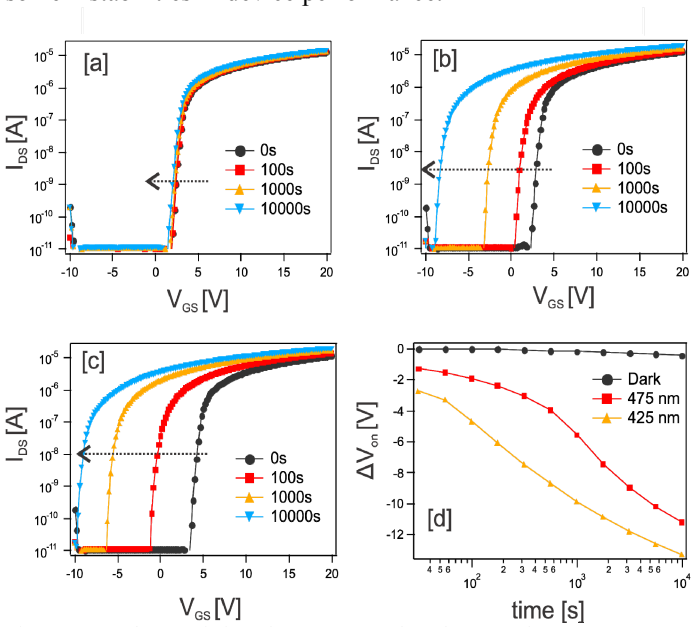


Fig 3: $I_{ds}$-$V_{gs}$ characteristics of PECVD ESL based TFT under NBIS. $V_{gs}$-$V_{on}$ = -14V. $V_{ds}$ = 0.5 V. [a] dark, [b] @475 nm illumination, [c] @425 nm illumination. [d] $\Delta V_{on}$ as a function of time

To elaborate on this, the impact of oxygen, hydrogen and water molecules on a-IGZO presented in literature should be discussed first. In [10] H incorporation in a-IGZO reduces the amount of oxygen vacancies but at the same time the Fermi level also moves into the conduction band which implies that the TFT will be completely on. When the sample is annealed the incorporated hydrogen becomes interstitial hydrogen and forms a complex with $V_O$. The TFT characteristics are recovered because of this but the deep subgap defects are also retrieved. On the other hand [11] show that increasing the amount of incorporated H increases the NBIS related instability due to formation of a hydrogen-related complex. More $O_2$ in a-IGZO reduces the deep traps caused due to oxygen vacancy related defects [12]. In our devices, the PECVD ESL is a source of $H_2$ which leads to doping of a-IGZO after ESL deposition [13]. But annealing the sample gets rid of this and we recover transistor behavior. However, the near VBM states are also recovered and will have a huge impact on NBIS related $V_{TH}$ shift. On the other hand PVD $SiO_2$ doesn't degrade the device as it contains very less H% and as the deposition is done in presence of oxygen plasma, the passivation helps in reducing near VBM states [9]. As a result device B shows less shifts compared to device A.

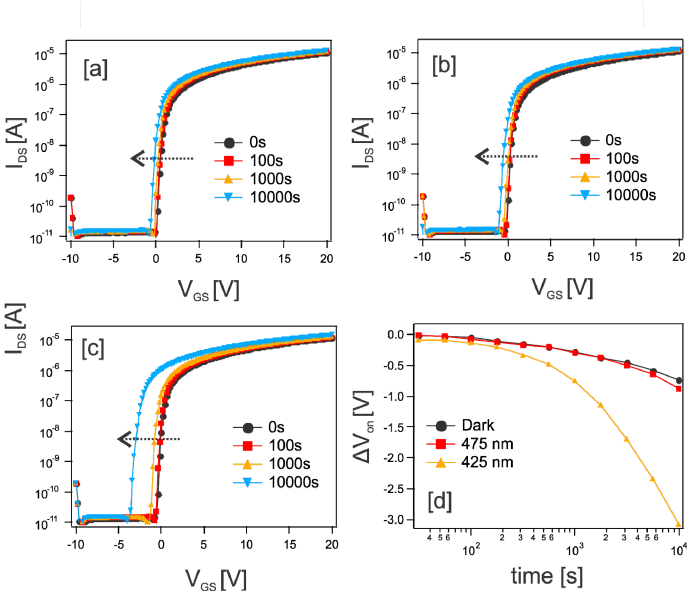


Fig 4: $I_{ds}$-$V_{gs}$ characteristics of PECVD ESL based TFT under NBIS. $V_{gs}$-$V_{on}$ = -14V. $V_{ds}$ = 0.5 V. [a] dark, [b] @475 nm illumination, [c] @425 nm illumination. [d] $\Delta V_{on}$ as a function of time

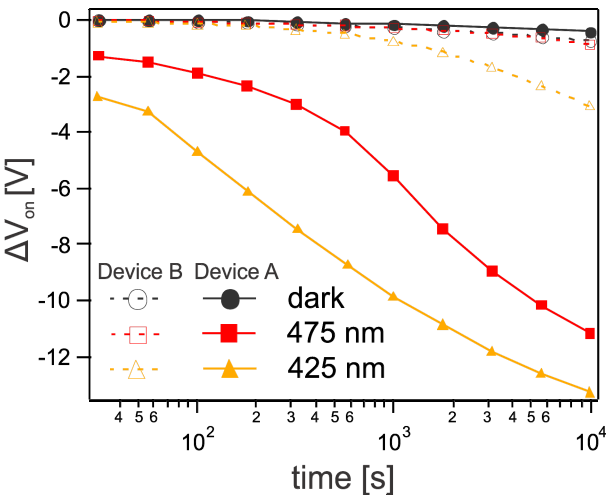


Fig 5: Comparison of $\Delta V_{on}$ of PECVD and PVD based ESL.
(full symbols + full lines) correspond to device A, (hollow symbols + dotted lines) correspond to device B.

## IV. SUMMARY

In summary, a comparison is made between PECVD and PVD ESL based TFTs. PVD ESL based TFTs show improved NBIS stability compared to PECVD ESL. This is due to reduction in near VBM trap states by PVD ESL. From a device point of view both PECVD and PVD ESL based devices show similar characteristics. However under NBIS, PVD ESL based TFTs show significantly improved stability.

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